REMARKS

This is a full and timely response to the non-final Office Action dated November 13, 2007. Claims 1-4, 6, 8-15 and 17-19 remain pending in the present application. Claims 1-4, 6, 8-11, 14-15 and 18 are amended as suggested in the Office Action to address the rejections under 35 U.S.C. §112, second paragraph. Claims 1, 9 and 15 are further amended. Support for the amendments can be found in the specification at least in paragraph 0010 and in FIGS. 1 and 2. Accordingly, no new matter is added to the application. In view of the foregoing amendment and the following remarks, reconsideration and allowance of the present application and claims are respectfully requested.

Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 1-4, 6, 8-15 and 17-19 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Applicant has amended claims 1-4, 6, 8-11, 14-15 as suggested in the Office Action to address the rejections under 35 U.S.C. §112, second paragraph. Applicant respectfully submits that claims 1-4, 6, 8-15 and 17-19 are in compliance with 35 U.S.C. § 112, second paragraph, and respectfully request that the rejection be withdrawn.

Rejections Under 35 U.S.C. § 103

Claims 1-4, 6, 8-15 and 17-19 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent Application Publication No. 2003/0035473 to Takinosawa (hereafter *Takinosawa*) in view of U.S. Patent No. 6,115,763 to Douskey *et al.* (hereafter *Douskey*) and further in view of U.S. Patent No. 5,956,370 to Ducaroir *et al.* (hereafter *Ducaroir*). For a claim to be properly rejected under 35 U.S.C. § 103, "[t]he PTO has the burden under section 103 to establish a *prima facie* case of obviousness. It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988) (Citations omitted). Further, "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification

obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266, 23 U.S.P.Q.2d 1780 (Fed Cir. 1992).

Takinosawa discloses a test circuit for a universal serial bus (USB) interface that includes a BIST circuit which allows for external data to be input during a self-test operation, and which allows for isolation of the transmitter section and receiver section during the self-test operation. *See Takinosawa*, paragraph 0009. Further, the BIST circuit in *Takinosawa* includes two different BIST circuits, a TX-BIST circuit 35 and a BIST analyzer circuit 49. These two different circuits are activated by different control signals. The TX-BIST circuit 35 is activated by the TX BIST enable signal and the BIST analyzer circuit 49 is activated by the RX BIST enable signal. *See Takinosawa*, FIG. 2 and paragraph 0037.

Importantly, the Office Action states that *Takinosawa* does not explicitly teach "a plurality of SERDESs," "a plurality of functional identical testers", or that "each said tester is connected to a common test bus that is integrated with said SERDESs and said testers."

The Office Action then relies on *Douskey* to partially remedy *Takinosawa* and states that *Douskey* teaches in an analogous art integrated circuit device 50 that generally includes "a plurality of cores 60 (a plurality of SERDESs and a plurality of functionally identical testers)" interconnected together via one or more functional interfaces. The Office Action then continues stating "*Douskey* suggests that the invention should not be limited to use with any particular design or end use of an integrated circuit device and that a core may be custom designed for a particular design, or may be reused from a previous design." The Office Action then states that "*Douskey* further teaches 'each said tester is connected to a common test bus that is integrated with said SERDESs and said testers' in that a service interface 55 for providing service functions (See col. 6, l. 65 to col. 7, l. 16) generally includes a bus 56 (common test bus) which couples a master interface unit (MIU) 58 (I/O tester controller of claim 6) to a plurality of core interface units (CIUs) 62 (said testers) disposed in each of cores 60."

The invention of *Douskey* relates to a "system on a chip." This is described in the second paragraph of the patent. *See Douskey*, col. 1, lines 17 to 33. A "system on a chip" may include a microprocessor, a memory, a bus interface and a memory controller. Advances in chip density permit all of these functions to be integrated onto the same integrated circuit device. FIG. 2 of *Douskey* illustrates a "system on a chip." Each core (60) may provide one

of the functions of the "system on a chip." As described in col. 6, lines 32 to 42 of *Douskey*, the different cores may be a processor core, and embedded memory, and input/output interface core, a memory interface, *etc.*

The Office Action then states that *Takinosawa* in view of *Douskey* does not explicitly teach "a bit error rate for each said SERDES is individually identified." The Office Action then relies on *Ducaroir* to provide this feature. The Office Action states that *Ducaroir* "teaches in an analogous art 'a bit error rate for each said SERDEs is individually identified' in that the BIST unit may optionally provide an error output signal to indicate when the sent and received data do not match, and an error counter and error trace buffer may be used to help identify the nature of the error and the bit error rate." The Office Action then states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify *Takinosawa's* built-in self test circuit (TX-BIST) circuit 35 to incorporate *Ducaroir's* error counter and error trace buffer. The Office Action states that the artisan would have been motivated to do so because it would enable *Takinosawa's* built-in self test circuit (TX-BIST) circuit 35 to identify the nature of an error and a bit error rate.

Ducaroir discloses a wrapback self test system in an input/output (I/O) interface device integrated into an integrated circuit to permit early detection of I/O interface defects during its manufacture, or prior to assembly of the integrated circuit onto a board, and to enable wrap back fault detection at an intra-chip resolution. *See Ducaroir*, col. 4, lines 48-54. *Ducaroir* continues stating "test data may be supplied to the transmitter portion of the I/O interface either externally or by test data stored in a built-in self tester (capital BIST). The BIST may optionally provide an error output signal to indicate when the sent and received data to not match, and an error counter and error trace buffer may be used to help identify the nature of the error and the bit-error rate." *See Ducaroir*, col. 5, lines 50-58. From this it is clear that *Ducaroir* merely describes a wrap back test system for an integrated I/O interface core of an integrated circuit.

From the language in the Office Action, it is clear that a *prima facie* case of obviousness exists only if *Douskey* teaches that the cores of *Douskey* include a plurality of SERDESs and a plurality of functionally identical testers, and if *Ducaroir* teaches a bit error rate being individually identified for each of a plurality of SERDESs.

Applicant has carefully reviewed *Douskey* and *Ducaroir* and can find no support for

concluding that the cores of *Douskey* include a plurality of SERDESs. Nor can the Applicant find support for concluding that *Ducaroir* discloses individually determining a bit error rate for a plurality of SERDESs.

As previously noted, *Douskey* teaches a "system on a chip." The cores may include a processor core, and embedded memory, and input-output interface core, and a memory interface. *See Douskey*, col. 6, lines 32 to 35. The only references to SERDESs appear to be in claim 42 of *Douskey* and in claim 8, lines 1 to 9. Generally, a core interface unit (CIU) is close to its associated core. Thus, for cores that are located far from the master interface unit (MIU), it may be desirable to serialize the CIUs coupling to the bus (74). This is shown at serial line (78) in figure 3 of *Douskey*. It may be desirable for relatively long runs of the bus (74) to be serialized so that the number of conductive traces routed over the long run is minimized. As shown in FIG. 3 of *Douskey*, the SERDESs are not within the CIU (88). Equally importantly, the SERDESs of *Douskey* are not tested. That is, the "testers" of *Douskey* are not enabled to detect performance characteristics of individual SERDESs, as set forth in Applicant's claim 1.

If it is asserted that *Douskey* indeed explicitly teaches SERDESs within the core (60), Applicant requests citation of the explicit teaching within *Douskey*. On the other hand, if it is asserted that a plurality of the cores inherently include SERDESs, Applicant respectfully disagrees. A person of ordinary skill in the art would recognize that it is not inherent to require recurring serialization and deserialization when a processor core accesses information from a memory core via a memory interface core.

Applicant respectfully asserts that since none of *Takinosawa*, *Douskey* or *Ducaroir* disclose, teach or suggest a plurality of SERDESs and a plurality of functionally identical testers connected to individually test the bit error rate of each SERDES, a *prima facie* case of obviousness is not established by the proposed combination.

Applicant respectfully submits that amended claims 1, 9 and 15 recite features that are not disclosed, taught or suggested by the proposed combination. Applicant respectfully submits that the proposed combination fails to disclose, teach or suggest at least "a plurality of functionally identical testers integrated with said plurality of SERDESs and said core processing logic, said testers being connected to individually test each of said plurality of SERDESs, each of said testers being enabled to detect performance characteristics of an

individual one of said plurality of SERDESs independently of other said testers and concurrently with said plurality of SERDESs, ***wherein a bit error rate for each of said plurality of SERDESs is individually identified***, and ***wherein said testers perform loop-back testing, static data testing and dynamic data testing***," and "wherein each of said testers is connected to a common test bus that is integrated with said plurality of SERDESs and said testers, ***said common test bus being separate from a data bus***, each of said testers having a unique address that enables independent accessibility of each of said testers via said test bus, said test bus being dedicated to providing signaling for said enablement to detect performance characteristics of said individual one of said plurality of SERDESs and further comprising a built in self-test (BIST) state machine integrated with said plurality of SERDESs and said testers, said BIST being connected to said test bus and being configured to sequence test operations by each of said testers," as recited in amended claim 1.

Applicant respectfully submits that the proposed combination fails to disclose, teach or suggest at least "a plurality of functional test interfaces (FTIs) integrally formed with said substrate, each of said FTIs being uniquely associated with a one of said SERDESs and being connected to said parallel data inputs and outputs of said associated one of said SERDESs, ***each of said FTIs being enabled to individually and concurrently test performances of each of said plurality of SERDESs wherein a bit error rate for each of said plurality of SERDESs is individually identified, and wherein said FTIs perform loop-back testing, static data testing and dynamic data testing***," and "an input/output controller (IOC) and common test bus integrally formed with said substrate, said common test bus being dedicated to providing signaling for enablement of testing, ***said common test bus being separate from a data bus***, said IOC being connected to each of said FTCs via said common test bus to transmit individually addressed commands to each of said FTCs, said IOC further being connected to exchange signals with an external device," as recited in amended claim 9.

Applicant respectfully submits that the proposed combination fails to disclose, teach or suggest at least "embedding a plurality of test interfaces within said integrated circuit such that each of said test interfaces is specific to a one of said SERDESs with respect to exchanging parallel data, including forming each of said test interfaces to include a test pattern generator connected to parallel data inputs of said SERDESs to which each of said test interfaces is specific and further including forming each of said test interfaces to include an

error detector to receive parallel data from said SERDESs to which said test interface is specific, ***wherein each of said SERDESs is individually and concurrently tested and a bit error rate of each of said SERDESs is individually identified, and wherein said testers perform loop-back testing, static data testing and dynamic data testing***," and "embedding an input/output controller (IOC) and a test bus within said integrated circuit, including connecting said IOC between said integrated circuit output and said test bus and ***including linking each said test controller to said test bus, said test bus being separate from a data bus***," as recited in amended claim 15.

Further, Applicant respectfully submits that claims 2-4, 6 and 8, which depend either directly or indirectly from allowable claim 1; claims 10-14, which depend either directly or indirectly from allowable claim 9; and claims 17-19, which depend either directly or indirectly from allowable claim 15, are allowable for at least the reason that they depend from allowable independent claims. *In re Fine, supra.*

CONCLUSION

Should the Examiner have any comment regarding the Applicant's response or believe that a teleconference would expedite prosecution of the pending claims, Applicant requests that the Examiner telephone Applicant's undersigned attorney.

Respectfully submitted,

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